LINEAR FULL-RATE PHASE DETECTOR AND CLOCK AND DATA RECOVERY CIRCUIT

ABSTRACT OF THE DISCLOSURE

Method and apparatus for recovering a clock and data from a data signal. One method of the invention includes receiving the data signal having a first data rate and receiving a clock signal having a first clock frequency, and alternating between a first level and a second level. The data signal is stored when the clock signal alternates from the first level to the second level, and the stored data signal is provided as a first signal a first amount of time later. The first signal is stored when the clock signal alternates from the first level to the second level, and the stored first signal is provided as a second signal a second amount of time later. A third signal is provided by delaying the first signal for a third amount of time. The third signal is stored when the clock signal alternates from the second level to the first level, and the stored third signal is provided as a fourth signal a fourth amount of time later. A fifth signal is provided by delaying the data signal a fifth amount of time. An error signal is generated by taking the exclusive-OR of the first and fifth signals; and a reference signal is generated by taking the exclusive-OR of the second and fourth signals. The first data rate is equal to the first clock frequency.